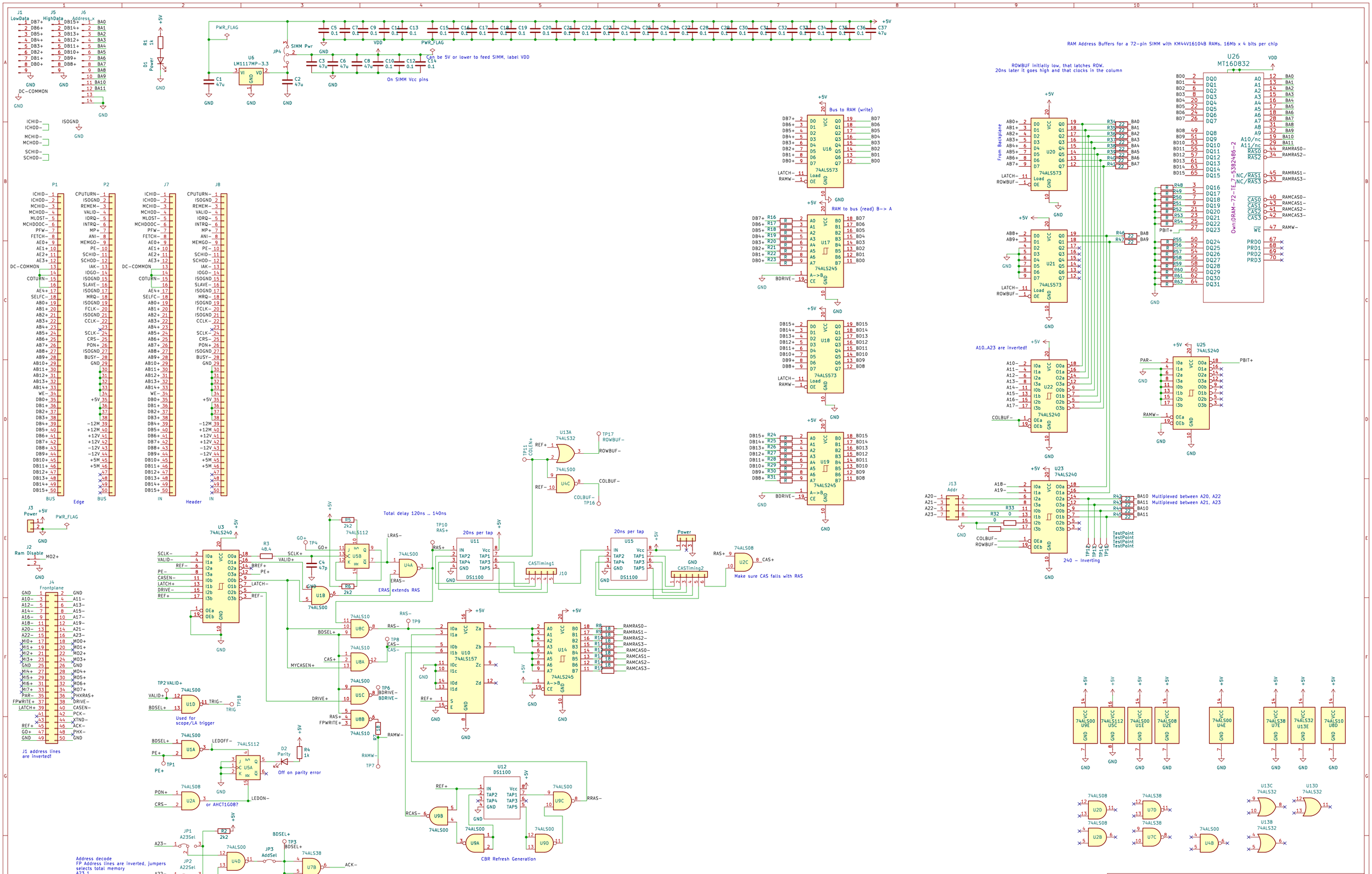
RAM Address Buffers for a 72-pin SIMM with KM44V16104B RAMs, 16Mb x 4 bits per chip
ROWBUF initially low, that latches ROW.
20ns later it goes high and that clocks in the column
U26
MT16D832
U16
74ALS573
U17
74ALS245
U18
74ALS573
U19
74ALS245
U20
74ALS573
U21
74ALS573
U22
74ALS240
U23
74ALS240
U25
74ALS240
U3
74ALS240
U14
74ALS245
U12
DS1100
U11
DS1100
U15
DS1100
U6
LM1117MP-3.3
U13A
74ALS32
U4C
74ALS00
U4A
74ALS00
U5B
74ALS112
U1B
74ALS00
U8C
74ALS10
U8A
74ALS10
U1C
74ALS00
U8B
74ALS10
U1D
74ALS00
U1A
74ALS00
U5A
74ALS112
U2A
74ALS08
U4D
74ALS00
U7B
74ALS38
U7A
74ALS38
U2C
74ALS08
74ALS157
U9B
74ALS00
U9A
74ALS00
U9C
74ALS00
U9D
74ALS00
U2D
74ALS08
U2B
74ALS08
U7D
74ALS38
U7C
74ALS38
U4B
74ALS00
U13C
74ALS32
U13D
74ALS32
U13B
74ALS32
U9E
74ALS00
U5C
74ALS112
U1E
74ALS00
U2E
74ALS08
U4E
74ALS00
U7E
74ALS38
U13E
74ALS32
U8D
74ALS10
Bus to RAM (write)
RAM to bus (read) B-> A
From Backplane
A10..A23 are inverted!
Multiplexed between A20, A22
Multiplexed between A21, A23
240 - Inverting
Total delay 120ns .. 140ns
20ns per tap
Make sure CAS falls with RAS
ERAS extends RAS
Used for scope/LA trigger
Off on parity error
CBR Refresh Generation
Address decode
FP Address lines are inverted, jumpers selects total memory
A23 1
A22 1 = 8M
A23 1
A22 3 = 16M
A23 3
A22 3 = 32M
J1 address lines are inverted!
Pedago Interaktiv AB
Sheet: /
File: HP1000RAM_SIMM_Buffers_20241130.kicad_sch
Title: HP1000 A400 RAM board - SIMM Data & Address Buffers
Size: A2
Date: 2024-12-28
Rev:
KiCad E.D.A. 8.0.2
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